LAB EXERCISE 5.1
Set-Clear Flip-flops

Objectives

This lab exercise will focus on the Set-Clear flip-flops. You will study several methods of implementing the S-C flip-flops.

Materials

LD-2 Logic Designer

74LS02 Quad 2-Input NOR IC

74LS00 Quad 2-Input NAND IC

Jumper Wires

TTL Data Book

Procedure

Until now we have concentrated on learning the basics of flip-flop operation. To better understand these experiments some nuances of flip-flops must be understood. Most of the flip-flops discussed in the text were level or pulse triggered devices. These devices use the standard flip-flop notations. As was noted in the text active LO inputs to the flip-flops are designated by a bubble on the input pin. Another type of flip-flop which operates similarly is the edge triggered flip-flop. These devices will have the same basic truth table as the devices we have studied; however, the output will change states only on the positive (LO to HI) or negative (HI to LO) edge of the clock pulses. Edge triggered inputs are shown by a triangle on the affected input as shown in Figure 5-15.

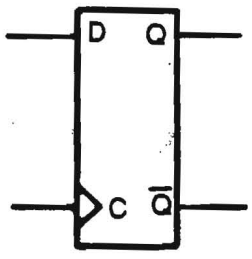


FIGURE 5-15. Schematic Symbol for Edge Triggered Flip-flop.

Circuits to accomplish the edge triggering functions are shown in Figure 5-16.

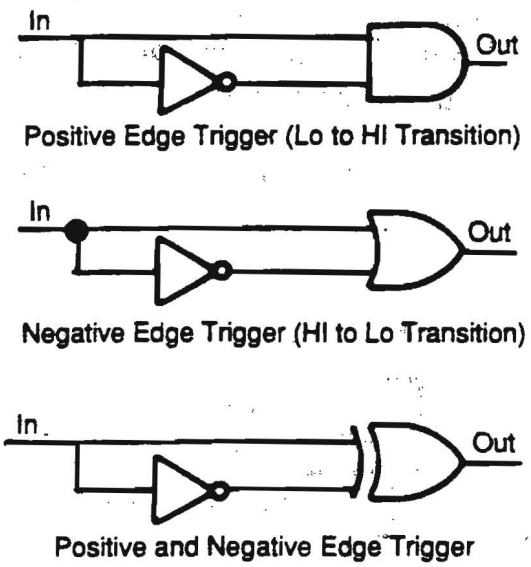


FIGURE 5-16. Edge Trigger Circuits.

The operation of the circuits is possible because of the gate delay of the inverters. This gate delay results in a short duration pulse corresponding to the edge of the clock pulse. With these fundamentals you are ready to perform experiments with flip-flops.

1. Wire the circuit shown in Figure 5-17 using the 74LS02 NOR gate.

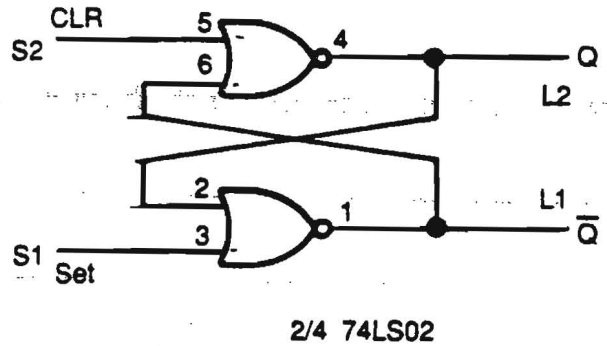


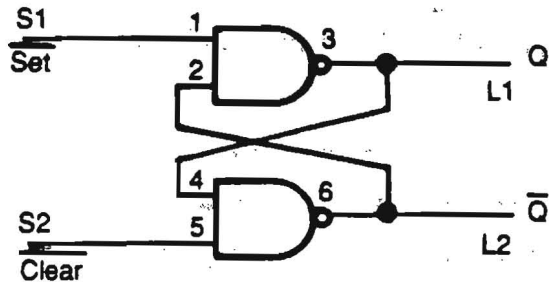
FIGURE 5-17. Schematic for NOR "S-C" Flip-flop.

2. Wire the power and ground pins to the 74LS02 if you have not already done so. Place S1 and S2 to OFF.

3. S1 is the Set input, S2 the Clear input, L2 the Q output and L1 the $\overline{Q}$ output. Determine the truth table for this circuit and record your result here.

4. Wire the circuit for the NAND S-C flip-flop shown in Figure 5-18.

FIGURE 5-18. Schematic for NAND "S-C" Flip-flop.



2/4 74LS00

5. Wire power and ground to the 74LS00. Place S1 and S2 to ON.

6. Turn on power. D1 and L2 should light.

7. Use S1, S2, L1 and L2 to determine the truth table for this circuit. Record your observations here.

8. Remove power from this circuit and leave the circuit on the circuit board for use in the next experiment.

Questions

1. Which states cause trouble for the NOR S-C flip-flop?

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2. Which states cause trouble for the NAND S-C flip-flop?

_____

_____

3. What state should the inputs to a NOR S-C flip-flop be in?

_____

4. What state should the inputs to a NAND S-C flip-flop be in?

_____

LAB EXERCISE 5.2
The "D" Latch

Objectives

In this lab exercise you will study the "D" latch. You will implement two types of "D" latches, one with active HI input and the other with active LO input.

Materials

LD-2 Logic Designer

74LS00 Quad NAND IC

74LS04 Hex Inverters IC

Jumper Wires

TTL Data Book

Procedure

1. Wire the active HI "D" latch circuit shown in Figure 5-19 using the 74LS00 and 74LS04 ICs. If you have retained the circuit from laboratory 5-1, this will only require rewiring the two input lines to the S-C FF.

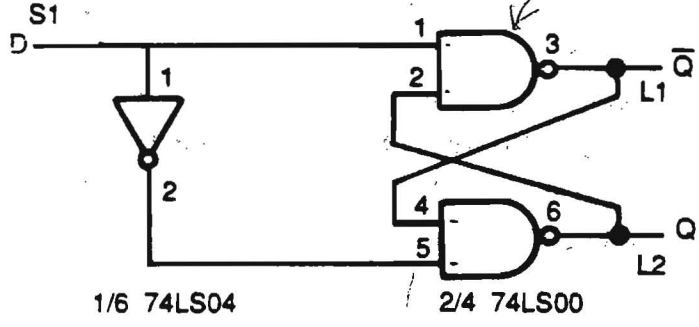
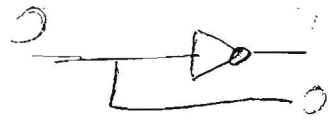


FIGURE 5-19. Schematic for "D" Flip-flop.



2. Wire power and ground to all circuits.

3. Use S1 as the D input, L2 as the Q output, and L1 as the complement output. Construct a truth table for this circuit.

4. Now, turn off power and swap the wires connected to pins 1 and 5 of the 74LS00. This will result in a low active "D" latch.

5. Use S1, L2 and L3 to determine the truth table for this circuit. Record your observations here.

6. Leave this circuit connected while you answer the following questions.

Questions

1. What do you notice about the circuit of Figure 5-19? How could this circuit be simplified?

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2. How could the circuit of step 5 be constructed using only one IC? Build a circuit to test your solution.

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LAB EXERCISE 5.3
The Clocked Set-Clear Flip-flops

Objectives

In this lab exercise we will study the clocked S-C flip-flops and clock signals.

Materials

LD-2 Logic Designer

74LS00 IC

Jumper Wires

TTL Data Book

Procedure

In order to perform this experiment we will need to understand something about clock signals. Clock signals are periodically spaced binary pulses. These pulses are used for circuit timing in sequential logic circuits. The duty cycle of a clock signal is the pulse length divided by the period and is expressed as a percentage by multiplying the quotient by 100. Two clock outputs are available on the LD-2 at the left most two-row breadboard.

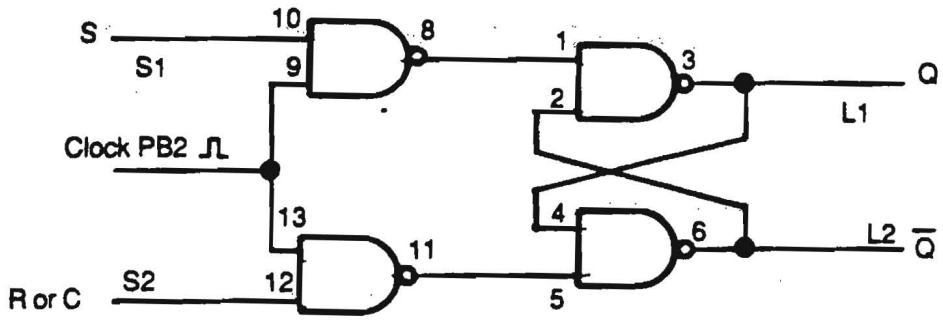
1. Connect the clock output to L7 on LD-2. Turn on power.

2. Set the clock frequency to 1 Hz.

3. Turn on power and observe L7. Record your observation. If an oscilloscope is available observe the clock pulse and sketch your observations.

4. Turn-off power and wire the circuit shown in Figure 5-20.

FIGURE 5-20. Schematic for Clocked "S-C" Flip-flop.



5. Use S1 as the Set input, S2 as the Clear or Reset input, PB2 for the clock input, L1 as the Q output, and L2 as the $\overline{Q}$ output to construct a truth table for this circuit. Record your observations here.

6. Record your observations of the outputs if the clock input is not actuated.

Questions

1. Does adding the clock circuitry cure the inherent flaws of the S-C flip-flop circuit? Explain.

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_____

_____

2. When do the input signals have an effect on the output states?

_____

_____

_____

LAB EXERCISE 5.4
The "T" Flip-flops

Objectives

In this lab exercise we will study the implementation and application of "T" flip-flops.

Materials

LD-2 Logic Designer

74LS74 Dual "D" Type Positive Edge Triggered Flip-flop With Preset and Clear

Jumper Wires

TTL Data Book

Procedure

1. Use the 74LS74 IC to construct the circuit shown in Figure 5–21.

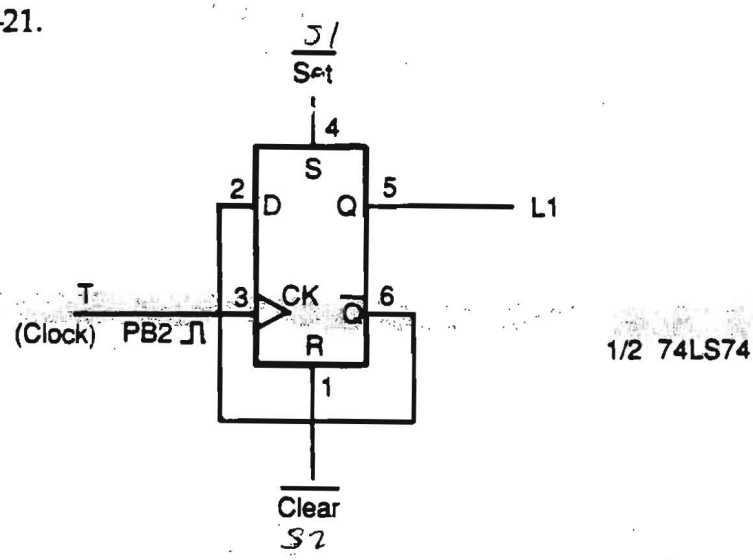

FIGURE 5-21. Schematic for "T" Flip-flop.

2. The feedback of the complement output to the D input results in the toggle operation. Wire power and ground to the IC.

3. Turn on power and record the initial state of the latch.

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4. Record your observation of L1, Q, and L7, clock, while pressing PB2 several times.

5. Turn Off power. Remove the wire to PB2 and place it on

the clock signal. Set clock frequency to 1 Hz.

6. Turn On power and observe the clock and "T" flip-flop outputs on L7 and L1 respectively. Record your observation here.

7. Leave this circuit connected while answering the following questions.

Questions

1. What effect does the "T" flip-flop have on binary pulse trains?

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2. In Step 4 how many times do you have to push PB2 before the flip-flop output toggles through an entire cycle (example: starts LO goes HI, then end LO)?

LAB EXERCISE 5.5
The Clocked "D" Flip-flops

Objectives

In this lab exercise you will study clocked "D" flip-flops.

Materials

LD-2 Logic Designer

74LS74 Dual "D" Type Positive Edge Triggered Flip-flop With Preset and Clear

Jumper Wires

TTL Data Book

Procedure

1. Wire the circuit shown in Figure 5-22 using the 74LS74.

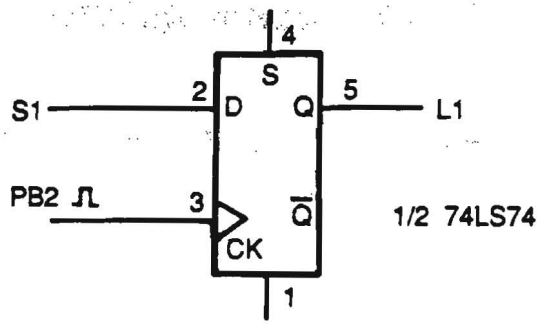

FIGURE 5-22. Schematic for Clocked "D" Flip-flop.

2. Wire power to the IC and place S1 to off.

3. Use S1 as the D input, PB2 as the clock input and L1 as the Q output and create a truth table for the clocked "D" flip-flop. Record this truth table here.

4. Use PB2 to determine on which edge of the clock pulse the "D" latch changes state.

_____

5. Remove power from the circuit and disassemble it.

Questions

1. From the results of step 4 describe the switching action of the 74LS74.

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2. Is this an active HI or active LO circuit?

_____

LAB EXERCISE 5.6
The "J-K" Flip-flops

Objectives

In this lab exercise you will study the "J-K" flip-flop and its applications.

Materials

LD-2 Logic Designer

74LS76 Dual J-K Flip-flop With Preset and Clear

74LS04 Quad Hex Inverters

Jumper Wires

TTL Data Book

Procedure

1. Wire the circuit shown in Figure 5-23 using the 74LS76 IC. Leave room on the breadboard for the 74LS04 IC.

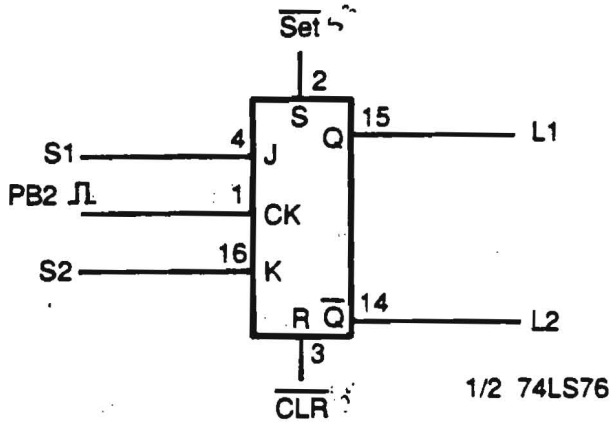

FIGURE 5-23. "J-K" Flip-flop Schematic.

2. Wire power and ground to this circuit. Place S1 and S2 to Off. Wire Set and Clear to +5 VDC.

3. Turn on power. Observe the initial state of the latch.

4. Use S1, S2, PB2 with L1 and L2 to make a truth table for the "J-K" flip-flop.

5. Place S1 and S2 to the high state. Turn off power. Connect the wire at PB2 to the clk signal of the LD-2 and tp L7.

6. Turn on power. Observe the clock on L7 and the FF output on L1. Describe your observations.

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_____

7. Turn off power. Wire the circuit shown in Figure 5-24.

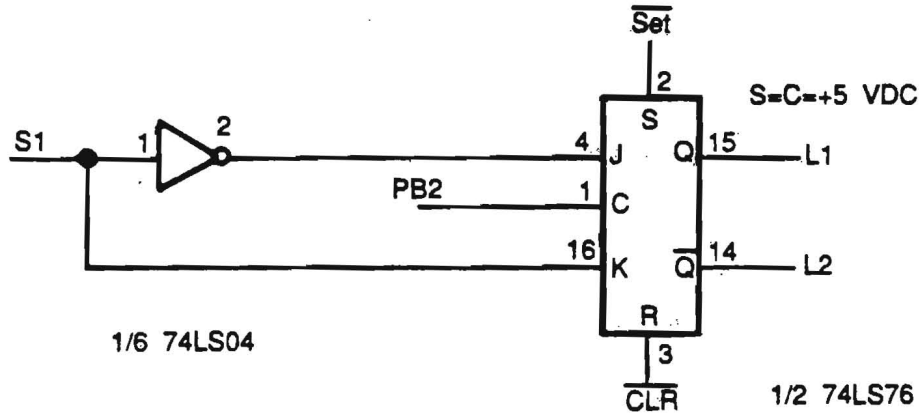

FIGURE 5-24. Schematic for Step Seven.

8. Wire power and ground to these circuits. Use S1, L1 and L7 to make a truth table for this circuit.

9. Leave this circuit connected while answering the following questions.

Questions

1. If both J and K inputs are held HI as in steps 5 and 6 what function is the J-K flip-flop performing?

_____

_____

2. What latch function does the circuit of step eight perform?

_____

_____

LAB EXERCISE 5.7
The One-shot

Objectives

In this laboratory you will learn about the monostable multivibrator or one-shot.

Materials

LD-2 Logic Designer

74121 Monostable Multivibrator With Schmitt-Trigger Inputs

Assorted Resistors

Assorted Capacitors

Jumper Wires

TTL Data Book

Procedure

1. Wire the circuit shown in Figure 5-25.

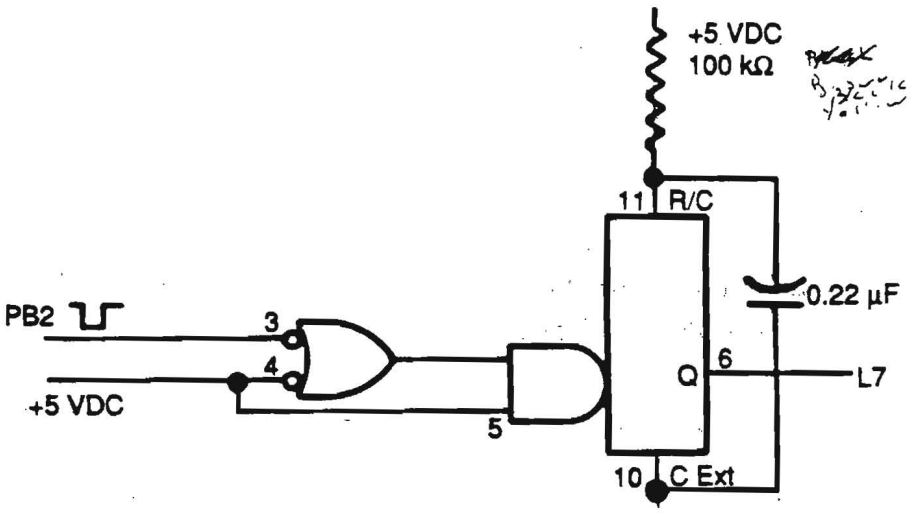

FIGURE 5-25. "One-shot" Schematic.

2. Wire power and ground to the circuit.

3. Turn on power. What do you notice about L7?

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_____

4. Press PB2. What happened to L7.

_____

5. Turn off power. Remove the 100 k ohm resistor and put a 47 k ohm resistor in its place.

6. Turn on power and press PB2. What did you observe? Compare this pulse with the pulse obtained in Step 4.

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7. Turn off power to this circuit.

Questions

1. Name one use of a One-shot IC.

_____

_____

2. Explain the name One-shot.

_____

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